

TSI-1

1k x 1k Time-Slot Interchanger

1 Introduction

The last issue of this product brief was April 28, 2005. A change history is included in Section [7 Change History on page 6](#). Red change bars have been installed on all text, figures, and tables that were added or changed. All changes to the text are highlighted in red. Changes within figures, and the figure title itself, are highlighted in red, if feasible. Formatting or grammatical changes have not been highlighted. Deleted sections, paragraphs, figures, or tables will be specifically mentioned.

This document is a high-level description for the TSI-1 time-slot interchanger device. The features and functions of the device are listed and explained at a level intended to meet the needs of the system design and component selection processes. Any standards governing the operation of the device are referenced, and the level of compliance is stated as appropriate. Broad definitions of its intended applications are given.

1.1 Related Documents

More information on the TSI-1 is contained in the following documents:

- The TSI-1 Data Sheet contains all information relevant to the use of the device in a board design. Pin descriptions, register descriptions, dc electrical characteristics, timing diagrams, ac timing parameters, packaging, and operating conditions are included.
- The TSI-1 Scalable Time-Slot Interchanger System Design Guide describes how to design software and hardware to support the device in various applications. The initialization procedure as well as some fundamental test setups for loopbacks and pattern generation are also described.
- The TSI Family Selection Guide is intended to help customers select the best device(s) for their application(s). The various devices and their distinguishing features are summarized.

2 Features

- 1,024 input channels x 1,024 output channels nonblocking DS0 time-slot interchange fabric.
- 16 full-duplex, serial time-division multiplexer (TDM) concentration highway interfaces.
- Compatible with GCI, SLD interfaces.
- Data rate selection of 2.048 Mbits/s, 4.096 Mbits/s, 8.192 Mbits/s, or 16.384 Mbits/s per highway.
- Bit and byte offset to 1/4 bit resolution per highway.
- Frame integrity mode to ensure intact transfer of wide-band data (N x DS0, ISDN H-channels).
- Low-latency mode for minimum delay on voice channels.
- 16-bit synchronous microprocessor interface for access to connection data and device registers.
- IEEE[®] 1149.1 boundary-scan test port (JTAG).
- Pattern generation and checking for on-line system testing (pseudorandom bit sequence (PRBS), quasirandom signal sequence (QRSS), or user-defined byte).
- Low-power 1.5 V core power supply with 3.3 V digital I/O compatibility.
- 240-pin ball grid array (PBGAM1) package, 19 mm² with a 1.0 mm ball pitch.
- -40 °C to +85 °C industrial temperature range.

3 Applications

The TSI-1 is suited to a wide variety of small-to-medium sized DS0 TDM switch applications. It has sufficient capacity to support up to an OC-12 link containing 64 kbits/s channels; it can provide useful grooming, first-stage switching, loopback, and test access on high-density transmission port cards (e.g., OC-12, OC-3, and DS3). For example, for lower-density systems, with several T1 ports it can support all the DS0 switching needs for the entire system. Typical applications include the following:

- Central office TDM switch.
- Integrated access devices.
- Next-generation digital loop carriers.
- Digital cross connects.
- Remote access concentrators.
- Remote access servers.
- Voice/IP gateways.
- Multiservice access platforms.
- Wireless base stations.
- Terminal multiplexer.

4 Description

The TSI-1 time-slot interchanger (TSI) is a time/space switch with DS0 granularity. The fabric is a nonblocking structure with 1,024 input channels that may be interchanged to any of 1,024 output channels. The input and output channels are arranged on time-division multiplexed serial highways. The timing and structure of these highways complies with Agere Systems Inc. concentration highway interface (CHI) standard. Each CHI is independently programmed, and the output CHIs support multidriver busing. The CHIs have a programmable data rate (up to 16.384 Mbits/s) and frame offset. Transmit and receive configurations are also independently programmable. The TSI-1 is configured via a 16-bit synchronous microprocessor interface, which is used to control the connection data and to access the device's registers.

The TSI-1 supports a number of additional time-slot test and code substitution functions in addition to its primary switching role. These options are programmed in a similar fashion to normal connections, by setting special bits in the connection control store. A frame integrity mode ensures constant delay for bonded DS0 channels in applications that switch wideband data (i.e., N x DS0 or ISDN H-channels). Low-latency mode ensures minimal delay for voice circuits.

Figure 5-1 represents a high-level block diagram of the TSI-1.

5 Block Diagram

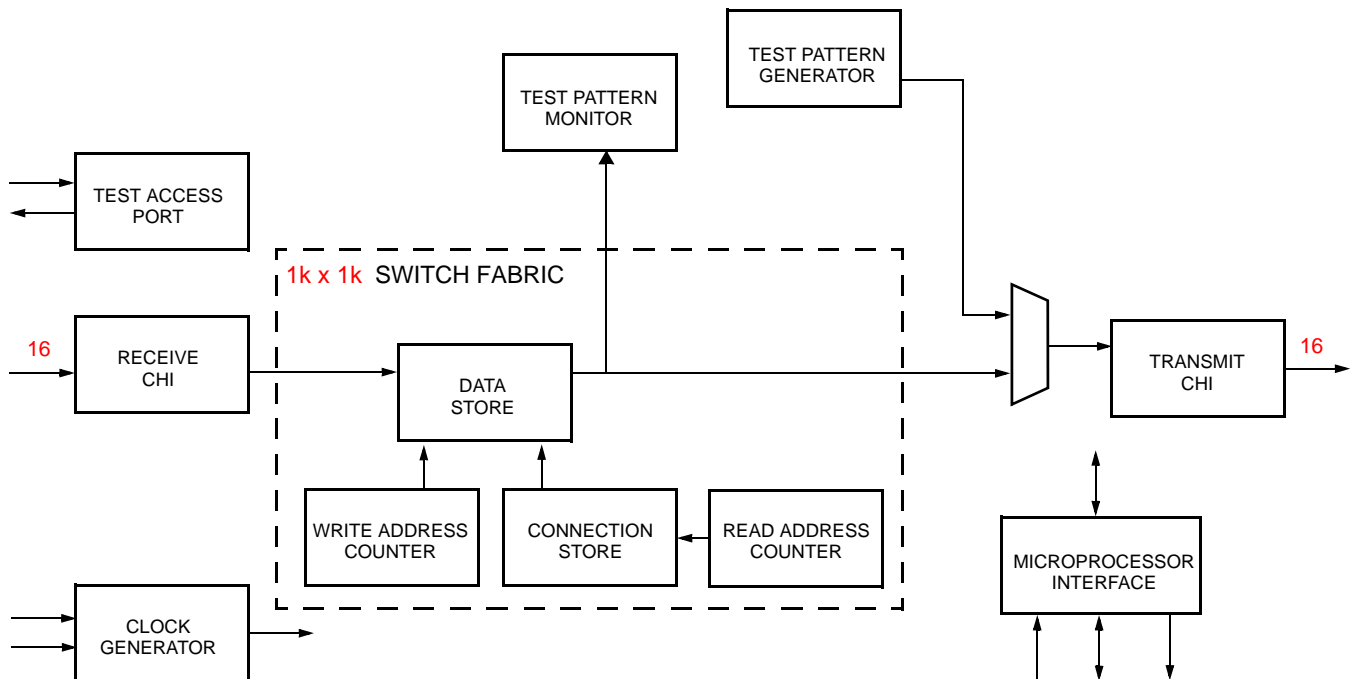


Figure 5-1. TSI-1 Block Diagram

5.1 Switch Fabric

The switch fabric performs the nonblocking switching function. It can switch any of the 1,024 possible incoming time slots to any of the 1,024 possible outgoing time slots. It uses the classic configuration of two memories, one containing the traffic data and the second containing the switching configuration. The switch fabric performs this switching function without regard to the physical link from which the time slot was taken; hence, the TSI-1 is a time-space switch. Time slots are rearranged in order within a frame (time) and among physical ports (space).

Time-slot data from the input TDM highways is converted to a common-rate parallel format by the CHI blocks. These data are written into the data store sequentially. The write address for the address for the data store is generated from the system clock (CHICLK) and frame synchronization (FSYNC) pulse. The clock is multiplied up to 164 MHz by a PLL in the clock generator block so that all 1,024 input time slots can be written into the data store during a 125 μ s frame. The entire switching operation from the input to output CHIs is synchronous to the CHICLK and frame locked to FSYNC.

Connections are established by programming the connection store. Each time slot on the output highways has an associated address in the connection store and each of those locations may be programmed with the input highway and time slot to which a connection is required. The connection store is also used to program all other per-time-slot options, such as frame integrity, translation table look-up, and test pattern insertion.

The switch fabric has the ability to select one of the following two latency modes for each connection:

- **Frame integrity.** Frame integrity mode ensures proper operation with wideband data by getting all of the time slots in an output frame from the same input frame.
- **Low latency.** Low-latency mode minimizes delay for voice applications.

The time-slot interchanger core is a memory-based implementation consisting of a data store and a connection store. The data store provides temporary storage for each of the 1,024 input TDM time slots. Received serial data is converted to parallel format, stored sequentially in the data store, and read to output time slots under control of data in the connection store. The connection store contains setup information for each of the 1,024 output time slots.

5.2 Microprocessor Interface

The TSI-1 has a versatile 16-bit microprocessor interface that provides access to its registers and connection store. It is designed to connect directly to the address and data buses of a synchronous general-purpose microprocessor and is compatible with *Motorola*®, *Intel*®, and other nonmultiplexed bus structures. The required microprocessor signals are as follows:

- 16-bit data bus (DATA[15:0]).
- 16-bit address bus (ADDR[15:0]).
- Four control lines (chip select (\overline{CS}), address strobe (\overline{AS}), read/write (R/\overline{W}), and data transfer acknowledge (\overline{DT})).
- A processor clock (MPUCLK).
- Interrupt output (\overline{INT}).

The connection store and device configuration registers are directly addressed.

The device generates interrupts on certain error conditions—illegal address, CHI timings errors, for example. These may all be masked individually.

5.3 Concentration Highway Interface (CHI)

The TSI-1 transmits and receives time-slot data by up to 16 transmit CHIs and 16 receive CHIs, which are single-ended serial TDM links. A programmable clock signal and a global frame synchronization pulse signal provide the required timing references to the CHI interface. The TSI-1 supports CHIs with unaligned framing; that is, each CHI's offset from the frame synchronization signal is independently programmable. Although the frame offsets can be different, they must be locked to a common frame reference. The transmit CHIs may be placed into the high-impedance (Hi-Z) state to allow busing of multiple drivers. Each CHI may be independently configured for direct connection to a variety of serial TDM interfaces operating at a variety of data rates, including GCI, SLD. Each CHI supports data rates of 2.048 Mbits/s (32 time slots), 4.096 Mbits/s, 8.192 Mbits/s, and 16.384 Mbits/s (256 time slots).

The receive CHI block reformats the serial CHI input data into a parallel format so that it can be written as 8-bit words into the data store. A 164 MHz clock is used for those transfers. This clock is derived using an internal phase-locked loop.

The transmit CHIs are similar in number, format, and flexibility to the receive CHIs. A parallel-serial conversion process is performed, and the time-slot data are slowed down from the 164 MHz internal clock rate to the required CHI output rate (2.048 Mbits/s, 4.096 Mbits/s, 8.192 Mbits/s, or 16.384 Mbits/s). The output CHI block also makes any time slot or bit offset adjustments that have been programmed.

5.4 CHI Frame Offset Selection

The device supports unaligned (but synchronous) TDM data streams. Each input CHI and each output CHI has a programmable offset (see Table 5-1) ranging from 0 to virtually a full frame. The TDM streams can be timed to align with the connecting device rather than having to be absolutely aligned with the TSI-1 frame synchronization input.

5.5 Test Pattern Generator and Monitor

The test pattern generator (TPG) and test pattern monitor (TPM) are a set of selectable test logic for support of transmission facility testing and maintenance. This block can supply and check any one of the test patterns defined in ITU-T O.150, O.151, or O.152, as well as user-defined patterns. Any combination of DS0s can be concatenated as a single broadband stream to test high-speed facilities. Additionally, the TPG/TPM provides the ability to perform diagnostic tests at both the system and device levels of operation.

System-level troubleshooting is facilitated with full narrowband/wideband test pattern generation and detection. Extensive device-level testing can quickly be performed with specialized test pattern generation and monitoring functions targeted at the CHI interface as well as the switch fabric itself. An effective self-test can be performed by configuring a test path and using the TPG/TPM and the internal loopback capabilities of the CHIs.

Test pattern generation and monitoring options are configured using the connection store. Only one type of test pattern can be transmitted at once, but it may be concatenated on any number of channels. The test pattern monitor may only check a single pattern on one time slot or wideband channel.

Table 5-1. Fractional Bit Offset Resolution

CHI Data Rate	CHICLK	Receive Offset Resolution	Transmit Offset Resolution
2.048 Mbits/s	8.192 MHz	1/4 bit (122.1 ns)	1/4 bit (122.1 ns)
2.048 Mbits/s	16.384 MHz	1/4 bit (122.1 ns)	1/4 bit (122.1 ns)
4.096 Mbits/s	8.192 MHz	1/4 bit (61.0 ns)	1/4 bit (61.0 ns)
4.096 Mbits/s	16.384 MHz	1/4 bit (61.0 ns)	1/4 bit (61.0 ns)
8.192 Mbits/s	8.192 MHz	1/4 bit (30.5 ns)	1/2 bit (61.0 ns)
8.192 Mbits/s	16.384 MHz	1/4 bit (30.5 ns)	1/4 bit (30.5 ns)
16.384 Mbits/s	16.384 MHz	1/4 bit (15.25 ns)	1/2 bit (30.5 ns)

5.6 Delay Through the TSI-1

For each connection written to the connection store, the switch fabric is set to operate in low latency mode or frame integrity mode. Low latency mode operates with minimum delay of a DS0 byte from an input to output time slot and is typically selected for voice applications. Frame integrity mode ensures intact switching of wideband data so that all the bonded time slots in one 125 μ s input frame are switched to the same 125 μ s output frame. Assuming the most favorable conditions, the minimum switch time (first bit in to first bit out) is two time-slot periods. The longest delay in low latency mode is about one frame plus three time slots. The longest delay in frame integrity mode is about three frames plus three time slots.

5.7 Clocks

Thehas two clock domains: one used for TDM data and the second used for the microprocessor interface. The input and output CHIs are in the TDM timing domain. The CHICLK input, which may be 16.384 MHz or 8.192 MHz, is the reference source for the TDM timing. Internally, this clock is multiplied up to 164 MHz for internal data transfer. An on-chip PLL is used for this purpose. An 8 kHz frame synchronization pulse is also required that must be synchronous with CHICLK. This is used as a reference for all the time-slot locations in the transmit and receive CHIs.

The second timing domain is used for the microprocessor interface. The MPUCLK input should be supplied along with the microprocessor data, address, and control signals. Typically, this is available as an output on most microprocessors, and is often referred to as the peripheral clock.

5.8 Reset

TheTSI-1 has a hardware reset input that is used to initialize various internal logic functions. This may be used during initialization and for device and board-level testing. A similar reset is available as a register bit to allow hardware reset under software control.

Note: Neither of these resets affects the contents of the data store, or more importantly, the connection store. However, the reset does put the device into a benign state (outputs high impedance or inactive).

6 Ordering Information

Device	Part Number	Ball Count	Package	Comcoe
TSI-1	TTSI001161BL-2-DB	240	PBGAM1	700085515
	L-TTSI001161BL-2-DB			700084937*

*Pb-free/RoHS

7 Change History

On page 1, changed the text (from 8 full-duplex to 16 full-duplex).

On page 3, made changes to Figure 5-1.

On page 4, changed the text in Section 5.3.

On page 5, changed the ordering information.

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